SOLE INVENTOR

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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Do-Young Lee a citizen of the Republic of Korea, residing at San 136-1, Ami-ri, Bubal-eub, Ichon-shi, Kyoungki-do 467-860, in the Republic of Korea have invented a new and useful CMOS IMAGE SENSOR IMPROVING PICTURE QUALITY, of which the following is a specification.

CMOS IMAGE SENSOR IMPROVING PICTURE QUALITY

Field of the Invention

The present invention relates to a CMOS image sensor and, more particularly, to an enhanced CMOS image sensor improving picture quality without quantization noise.

Background of the Invention

Generally, an image sensor is an image capture device that captures an image, for example, by using the photo-absorption characteristic of semiconductors, i.e., a photon reaction process. All objects in nature have luminance and color, and each pixel of an image sensor converts such photonic information to an electrical signal corresponding to the color and the luminance of the object. The image sensor processes the electrical signal(s) to create a high quality image of the object.

Normally, the image sensor is composed of a pixel array constructed with tens of thousands to hundreds of thousands of unit pixels, an A/D converter for converting an analog voltage to a digital value, and memory units. Some image sensors support a correlated double sampling technique (hereinafter, referred to as "CDS") in generating the high quality image. CDS is widely known technology.

The image signal generated from the image sensor has to be passed through various steps before a high quality image

is generated. The conventional image processing is described in accordance with Fig. 1

Fig. 1 is a flowchart illustrating the conventional image processor connected to a CMOS image sensor. As shown, an analog image signal is received from a pixel array and this is normally converted to an 8-bit digital image signal after the CDS process in the CMOS image sensor. The 8-bit digital image signal is modified using several signal processing steps to achieve better image quality. Gamma correction is one of these processing steps.

Unfortunately, when gamma correction is applied to the digitized image signal generated from the CMOS image sensor, the effective bit resolution of the image data is reduced from the original 8 bits to 5 or 6 bits image resolution.

Fig. 2 is a high-level block diagram illustrating components of a conventional CMOS image sensor. Detailed connections between blocks are omitted in Fig. 2, but would be understood. Both the A/D conversion and the CDS are now explained.

As shown in Fig. 2, an analog-to-digital converter (ADC) is composed of a ramp signal generator 10, a comparator 20, and a memory buffer 30. The ramp signal generator 10 makes a ramp signal, which is used as a reference signal to convert an analog image signal generated from pixel array into a digital value, or a digital image signal. The comparator 20 compares the analog pixel output signal from the pixel array with a reference ramp signal from the ramp signal generator

10. The memory buffer 30 saves the result of the comparison of the pixel output voltage level and the ramping voltage level, which drops little by little by a uniform voltage level at each digital clock pulse.

The ADC performs the analog-to-digital conversion using the following steps: applying the analog image signal from the pixel array to the comparator 20 as an input; applying the ramp signal generated from the ramp signal generator 10 as another input; and saving a clock count value to memory buffer 30, wherein the clock count value is the number of counted clock pulses until the ramping voltage level, which drops each clock pulse, goes through the pixel output voltage level. By way of further background on the analog-to-digital conversion steps, Fig. 3 shows a detailed illustration of how the digital data image may be created.

As mentioned above, it is necessary to have a ramp signal to perform the CDS. Fig. 4 shows a double ramp signal for the CDS, as would be created by the ramp signal generator 10. The ramp signal generator 10 makes a first ramp signal for reading a reset level that represents the initial state of a pixel in the pixel array. A second ramp signal is generated by the ramp signal generator 10 for reading the signal level of the pixel output. The ramp signal generator 10 outputs a linear ramping signal as shown Fig. 4.

Finally, since the gamma correction is performed with the digital data after the analog-to-digital conversion, the original 8-bit image quality is reduced to 6-bit image

quality, for example, by the characteristics of the digital gamma correction. This decreases the digital image signal and the image quality of the CMOS image sensor.

Summary of the Invention

It is, therefore, desirable to provide an enhanced CMOS image sensor that improves the entire image quality by concurrently performing gamma correction and analog-to-digital conversion of image signals, by modifying the ramp signal.

In accordance with an aspect of the disclosed, there is provided a CMOS image sensor, having: an image capturing unit for converting light incident upon a photo-sensitive area to an analog signal; an analog-to-digital converter for converting the analog image signal to a digital image signal; and a ramp signal generator for producing a ramp signal in order to provide a reference voltage signal to the analog-to-digital converter, the ramp signal generator including: a) a plurality of capacitors and switches; b) an amplifier coupled to the plurality of capacitors and switches for receiving gain and reset voltages from an external circuit; and c) a capacitance controlling unit coupled in parallel to at least one of the plurality of capacitors in the ramp signal generator in order to form the ramp signal for an analog gamma correction. The plurality of switches in the ramp signal generator are selectively operated in response to a

control signal from a digital controller in the CMOS image sensor.

Brief Description of Drawings

The above and other objects and features of the disclosed embodiments will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 is a flowchart illustrating image processing steps in a conventional CMOS image sensor;

Fig. 2 is a block diagram illustrating components of a conventional COMS sensor;

Fig. 3 is a circuit level diagram illustrating an analog-to-digital conversion in accordance with Fig. 2;

Fig. 4 is an exemplary diagram illustrating a ramp signal for performing the CDS in the conventional CMOS sensor with a line-based analog to digital converter;

Fig. 5 is a block diagram illustrating an analog-to-digital conversion and a gamma correction of image signals received from pixels in a CMOS image sensor in accordance with an embodiment of the disclosed apparatus;

Fig. 6 is an exemplary diagram illustrating a ramp signal for concurrently performing an analog-to-digital conversion and a gamma correction on image signals received from pixels in the CMOS image sensor in Fig. 5;

Fig. 7 is a detailed diagram of a chopper comparator in accordance with an embodiment of the disclosed apparatus;

Fig. 8 is a schematic diagram of a typical ramp signal generator; and

Fig. 9 is a detailed diagram of the ramp signal generator of Fig. 5 in accordance with the preferred embodiment of the disclosed apparatus.

Detailed Description of the Invention

As shown in Fig. 5, a CMOS image sensor has a comparator 100, a ramp signal generator 120, an up-counter (clock pulse counter) 140, a multiplexer 160 and a latch 180. The comparator 100 performs a CDS, an analog-to-digital conversion and a gamma correction of a ramp signal and an analog image signal received from pixels, for example, a pixel array. The ramp signal generator 120 generates a ramp signal, as shown in Fig. 6, in response to an external control signal for the gamma correction and outputs the ramp signal to the comparator 100. The up-counter 140 counts the number of counted clock pulse until the ramping voltage level, which drops in each clock pulse, goes through the pixel output voltage level. The multiplexer 160 selectively outputs a result of the up-counter 140 to an 8-bit latch, in response to an output signal of the comparator 100. The latch 180 saves an output of the multiplexer 160 and feeds a

latched value to another multiplexer as an input in response to the clock.

The comparator 100 is composed of the CDS performing unit 102 and a comparison unit 104. The CDS unit 102 performs the CDS on the analog image signal data received from pixels. The comparison unit 104 performs the gamma correction and the analog-to-digital conversion of the analog image signal to a digital image signal after the CDS step. The comparison unit 104 provides the result to the multiplexer 160.

Thus, the analog pixel output signal is connected to the CDS performing unit 102 in the comparator 100, and the CDS step is performed at the analog level, i.e., before the analog-to-digital conversion in the comparison unit 104.

Fig. 7 is a detailed schematic diagram of the comparator 100 for performing the CDS function at an analog level.

In operation, when receiving a reset level value for the CDS, an output signal Vout from the comparator 100 is in a middle voltage level because three switches S_1, S_3, and S_4 are closed, and a switch S_2 is opened. At this point, each device offset voltage is saved in two capacitors C_2 and C_3. Next, the switch S_2 is shorted and a difference between an initial state voltage of the ramp signal generator 120 and the pixel initial output voltage level is saved at a capacitor C_1. The pixel outputs the real image voltage level after the switches S_2, S_3, and S_4 are opened again. Next, the switch S_1 is opened, and then S_2 is closed. At that time, the voltage of the common node of the capacitors C_1 and C_2 shifts by the result

voltage of CDS. Finally, the state of the output Vout transits at the time the voltage of the common node of the capacitors C_1 and C_2 reverses to the initial voltage level after the ramp signal generated from the ramp signal generator 120 starts ramping.

In the meantime, the ramp signal generator 120 has to be designed to represent a gamma curve for simultaneously performing the gamma correction and the analog-to-digital conversion in the comparator 100 of Fig. 5. The size of the step voltage in a ramp signal generator is usually determined by the difference between a gain voltage V_Gain and a reset voltage V_RESET , as shown by the ramp signal generator exemplary shown in Fig. 8. Another parameter affecting the unit ramping step voltage in the ramp signal generator circuit of Fig. 8 is the ratio of capacitors C_4 and C_5. The relationship is represented by following equation.

$$V_1\ step \propto \frac{C_4}{C_5} \qquad \text{Eq. 1}$$

Fig. 9 shows the preferred ramp signal generator 120 for generating a ramp signal for concurrently performing the gamma correction and the analog-to-digital conversion in the comparator 100. The ramp signal generator 120 has: a switch S_9, switches S_{11} to S_{1n}, capacitors C_{11} to C_{1n}, a switch S_{10}, a switch S_{20}, a switch S_{21}, an amplifier AMP, a switch S_{reset}, and

a capacitor C_x. One of two terminals of the switch S_9 is connected to a gain voltage, V_Gain, and the other is connected to the plurality of switches S_{11} to S_{1n} in parallel. The switches S_{11} to S_{1n} are connected to the capacitors C_{11} to C_{1n}, respectively. The two terminals of the switch S_{10} are connected to the plurality of the switches S_{11} to S_{1n} and to a ground source, respectively. One of two terminals of the switch S_{20} is commonly connected to the plurality of capacitors C_{11} to C_{1n}, and the other is connected to a reset voltage, V_RESET. The switch S_{21} is commonly connected to the plurality of capacities C_{11} to C_{1n}. A negative input terminal of the AMP is directly connected to the switch S_{21}, and a positive input terminal is connected to the reset voltage, V_RESET. The AMP outputs a ramp signal Vramp capable of performing a gamma correction in the CDS. A switch S_{reset} and a capacitor C_x are connected in parallel between the negative input terminal and an output terminal of the AMP.

The ramp signal can be modified based on an amount of a capacitance of the capacitors C_{11} to C_{1n} by controlling the switches S_{11} to S_{1n} using control signals provided from a digital controller in the CMOS image sensor. Accordingly, modified various ramp signals can be obtained and used to perform a desired gamma correction, because the Eq. 1 may now be expressed as:

$$V_1\ step \propto \frac{C_{11}}{C_x} \quad \text{(when S11 is connected)} \qquad \text{Eq. 2}$$

$$V_1\ step \propto \frac{C_{12}}{C_x}$$ (when S12 is connected)

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$$V_1\ step \propto \frac{C_{1n}}{C_x}$$ (when S1n is connected)

Fig. 6 shows such a modified ramp signal for the gamma correction where a dotted line represents a normal ramp signal and a solid line represents the modified ramp signal. As is provided, the CMOS image sensor of the disclosed device can simultaneously perform the gamma correction and the analog-to-digital conversion.

As stated above, the enhanced CMOS image sensor of the disclosed device does not decrease the number of valid image bits. Accordingly, the now disclosed devices prevent the decrease of a picture quality caused by conventional gamma correction.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.